Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 0057-2362-2YY	SERIAL NO. New Application
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Shigenobu MAEDA, et al.	
		FILING DATE HEREWITH	GROUP

JC511 U.S. PTO 09/176315 10/22/98

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
SWC	AO	5-218426	08/27/93	Japan (with English Abstract)		X
	AP	62-193170	08/25/87	Japan (with English Abstract)		X
	AQ	2-280371	11/16/90	Japan (with English Abstract)		X
SWC	AR	8-64824	03/08/96	Japan (with English Abstract)		X
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

SWC	AW	S. MAEDA, et al., "Suppression of Delay Time Instability on Frequency Using Field Shield Isolation Technology For Deep Sub-Micron SOI Circuits", IEDM, 1996, pp. 129-132.
	AX	T. IWAMATSU, et al., "CAD-Compatible High-Speed CMOS/SIMOX Technology Using Field-Shield Isolation for 1M Gate Array", IEDM, 1993, pp. 475-478.
SWC	AY	T. IWAMATSU, et al., "High-Speed 0.5 μ m SOI 1/8 Frequency Divider With Body-Fixed Structure For Wide Range of Applications", SSDM, 1995, pp. 575-577
	AZ	

Examiner	CRANE	Date Considered	7/14/00

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.